

Seminar

SpringSoft Verification Enhancement Technologies & Debug Training

- Date: 23 Jun 2009 (Tuesday):
- Time: 10:00am – 4:30pm:
- Audience: Digital IC Design & Verification Engineers:
- Language: Mandarin:
- Venue: IC Training Centre, Unit 308D, 3/F, IC Development Centre,
No.6 Science Park West Avenue, Hong Kong Science Park, Shatin, N.T., Hong Kong.:

Free of Charge



Register Now!

Background

As Forerunner and Technical Leader in IC Debug Territory, SpringSoft delivers unique Automation Technologies that save time at key pain points in the Design and Verification of complex Digital ICs, ASICs, Microprocessors, and SoCs. Our solutions automate tedious, time-consuming tasks allowing you to spend more time adding value to your designs.:

Seminar Agenda

<i>Introduction to SpringSoft Verification Enhancement Technologies</i>	
10:00 am ~ 10:15 am	Opening: Introduction of SpringSoft
10:15 am ~ 11:15 am	Verdi Automatic Debug System for Design & Verification
11:15 am ~ 11:30 am	Break
11:30 am ~ 12:00 am	Siloti Visibility Enhancement Technologies
<i>Debug Practice from Different Views</i>	
1:30 pm ~ 1:40pm	Preparations Before Debugging
1:40 pm ~ 2:10 pm	View and Debug Source Code
2:10 pm ~ 2:30 pm	Debug Design Circuits with Hierarchical and Flatten Views
2:30 pm ~ 2:50 pm	Simulation Results Analysis in Waveforms
2:50 pm ~ 3:10 pm	Break
3:10 pm ~ 3:25 pm	Analyze Finite State Machines Graphically
3:25 pm ~ 3:55 pm	Total New Debug Way with Temporal Flow Views
3:55 pm ~ 4:15 pm	FSDB Applications
4:15 pm ~ 4:30 pm	Q&A

Seminar

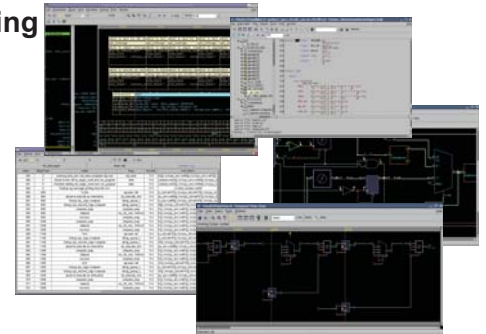
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About the Solutions

Verdi Automated Debug System

The Verdi Automated Debug System is an advanced solution for debugging your digital designs that cuts debug time by as much as 50%. The debug system:

- Automates tracing from effects to causes with its unique behavior analysis technology
- Unifies design comprehension across the following:
 - ◆ Abstraction levels - System, Testbench, RTL, Gate
 - ◆ Languages - Verilog, VHDL, SV, SVA, SVTB
 - ◆ Dynamic and Static Verification



Siloti Visibility Automation System

The Siloti Visibility Automation System transforms verification methodologies by eliminating the overhead associated with dumping data for all the signals in a design. The Siloti technology provides full visibility of internal signals for complex IC and system-on-chip (SoC) designs by identifying the minimal set of signals for dumping, generating "on-demand" the rest of the signal data, and correlating gate-level results to the register transfer level (RTL) source code. Siloti products are used during full-chip simulation, emulation and first-silicon prototyping to:

- Achieve full visibility with minimal impact on verification overhead using the Siloti on-demand data expansion engine
- Remove the guesswork of what signals to record with the Siloti essential signal analysis engine
- Slash file sizes, file transfer times and storage costs

For more information on Verification Enhancement Technologies, please refer to www.springsoft.com

For Register, Please contact: Maggie Li (maggie_li@springsoft.com) Tel: 86-21-54902090 Ext: 100



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* **Company Name:**

* **Name:**

* **Job Title:**

* **Email:**

* **Telephone:**

** required field*

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